

IN THE CLAIMS

Following is a complete set of claims. No changes have been made to the claims.

CLEAN VERSION OF THE ENTIRE SET OF CLAIMS

01 1. (TWICE AMENDED) A method comprising:  
2 pre-fetching a plurality of data from a memory to a data queue in response to a request;  
3 ~~and~~  
4 delivering the pre-fetched data from the data queue to a bus independently of the memory.

1 2. (AMENDED) The method of claim 1 wherein pre-fetching comprises:  
2 determining if an amount of data in the data queue is above a predetermined level; and  
3 placing the request to a memory controller controlling the memory if the amount of data  
4 is not above the predetermined level, the request causing the memory controller to transfer the  
5 plurality of data to the data queue, the request being buffered in a request queue.

1 3. (AMENDED) The method of claim 2 wherein the delivering comprises:  
2 transferring the data from the data queue to the bus if the data in the data queue is ready.

1 4. The method of claim 1 further comprising:  
2 determining if the request is valid; ~~and~~  
3 ~~processing a cache miss request if the request results in a cache miss.~~

1 5. The method of ~~claim 4 wherein the processing of the cache miss request~~  
2 ~~comprises:~~ *Claim 1 Further comprising*  
3 providing a purge signal; ~~and~~  
4 marking an entry in a scheduler according to the purge signal;  
5 ~~purging data corresponding to the marked entry, and~~  
6 ~~placing the request to the memory controller.~~

1           6.     The method of claim 6 wherein the bus is a peripheral component interconnect  
2 (PCI) bus.

1           7.     The method of claim 6 wherein the request is one of a 32-byte and a 64-byte  
2 requests.

1           8.     (TWICE AMENDED) An apparatus comprising:  
2           a pre-fetcher to pre-fetch a plurality of data from a memory to a data queue in response to  
3 a request;  
4           a queue controller coupled to the data queue and the pre-fetcher to deliver the pre-fetched  
5 data from the data queue to a bus independently of the memory.

1           9.     (AMENDED) The apparatus of claim 8 wherein the pre-fetcher comprises:  
2           a watermark monitor to determine if an amount of data in the data queue is above a  
3 predetermined level;  
4           a request packet generator coupled to the watermark monitor to place the request to a  
5 memory controller controlling the memory if the amount of data is not above the predetermined  
6 level, the request causing the memory controller to transfer the plurality of data to the data queue;  
7 and  
8           a request queue coupled to the request packet generator to store the request provided by  
9 the request packet generator.

1           10.    (AMENDED) The apparatus of claim 9 wherein the queue controller transfers the  
2 data from the data queue to the bus if the data in the data queue is ready.

1           11.    (AMENDED) The apparatus of claim 9 further comprising:  
2           a peripheral bus controller coupled to the bus and the pre-fetcher to determine if the  
3 request is valid;  
4           a data coherence controller coupled to the pre-fetcher to provide a purge signal when the  
5 request corresponds to a cache miss; and

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6 a scheduler coupled to the request queue and the data coherence controller to store entries  
7 corresponding to the request, the entries being marked according to the purge signal from the  
8 data coherence controller.

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1 12. (AMENDED) The apparatus of claim 11 further comprising:  
2 a data mover coupled to the data queue and the scheduler to transfer data from the  
3 memory to the data queue, the data mover purging data corresponding to a marked entry from the  
4 scheduler.

1 13. The apparatus of claim 12 wherein the bus is a peripheral component interconnect  
2 (PCI) bus.

1 14. The apparatus of claim 13 wherein the request is one of a 32-byte and a 64-byte  
2 requests.

1 15. (TWICE AMENDED) A system comprising:  
2 a memory;  
3 a bus; and  
4 a bus access circuit coupled to the memory and the bus to reduce latency in accessing the  
5 memory from the bus, the bus access circuit including:  
6 a pre-fetcher to pre-fetch a plurality of data from the memory to a data queue in  
7 response to a request, and  
8 a queue controller coupled to the data queue and the pre-fetcher to deliver the pre-  
9 fetched data from the data queue to the bus independently of the memory.

1 16. (TWICE AMENDED) The system of claim 15 wherein the pre-fetcher  
2 comprises:  
3 a watermark monitor to determine if an amount of data in the data queue is above a  
4 predetermined level;  
5 a request packet generator coupled to the watermark monitor to place the request to a  
6 memory controller controlling the memory if the amount of data is not above the predetermined

7 level, the request causing the memory controller to transfer the plurality of data to the data queue;  
8 and  
9 a request queue coupled to the request packet generator to store the request provided by  
10 the request packet generator.

1 17. (AMENDED) The system of claim 16 wherein the queue controller transfers the  
2 data from the data queue to the bus if the data in the data queue is ready.

1 18. (AMENDED) The system of claim 16 wherein the bus access circuit further  
2 comprises:  
3 a peripheral bus controller coupled to the bus and the pre-fetcher to determine if the  
4 request is valid;  
5 a data coherence controller coupled to the pre-fetcher to provide a purge signal when the  
6 request corresponds to a cache miss; and  
7 a scheduler coupled to the request queue and the data coherence controller to store entries  
8 corresponding to the request, the entries being marked according to the purge signal from the  
9 data coherence controller.

1 19. (AMENDED) The system of claim 18 wherein the bus access circuit further  
2 comprising:  
3 a data mover coupled to the data queue and the scheduler to transfer data from the  
4 memory to the data queue, the data mover purging data corresponding to a marked entry from the  
5 scheduler. 20. (AMENDED) The system of claim 19 wherein the bus is a peripheral component  
6 interconnect (PCI) bus.

1 20. The system of claim 19 wherein the bus is a peripheral component interconnect  
2 (PCI) bus.

1 21. The system of claim 20 wherein the request is one of a 32-byte and a 64-byte  
2 requests.